MOTOROLA
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68K ColdFire MICROPROCESSOR

Errata to
MCF5307 ColdFire® Microprocessor User's Manual

These errata describes corrections to the *MCF5307 ColdFire Microprocessor User's Manual*. For convenience, the section number and page number of the errata item in the user's manual are provided. The MCF5307 device referred to in this document is the MCF5307FTxxB. Please check the WWW at http://www.motorola.com/ColdFire for the latest updates.

Section #/Page #	Changes

2.6, 2-40

Add the following text:

Note that if the upper 16 bits of a longword aligned fetch location contain an unknown (illegal) opcode while the lower 16 bits contain a Bxx.B opcode (where Bxx = BRA, BSR, Bcc), an incorrect re-direction of the prefetch stream to an improper target location will occur. An example of this is seen in the following code:

```
      mov.l  (4,%pc,%d0.l*4),%a0
      jmp    (%a0)
label:
      long   label1
      long   label2
```

In this case, the code would disassemble to the following:

```
X-6:    207b 0c04  #mov.l
X-2:    4ed0       #jmp
X+0:    wxyz 6040  #pointer to label1 (example)
X+4:    .........  #pointer to label2
```

In this example, after the JMP instruction, the label pointer disassembles to what looks like an unknown opcode (wxyz = any unknown opcode) followed by a 16-bit opcode that looks like a Bxx.B opcode, but actually isn't. In this case, the branch acceleration logic calculates the target address and begins prefetching at X + 0x44. This can be particularly problematic if the address that the acceleration logic jumps to is at an offset range that doesn't exist, resulting in an illegal access. More specifically, if the 8-bit displacement that is decoded in the look-alike Bxx.b instruction branches to an offset (-128 byte to +128 byte) that no chip-select is programmed to or where no memory exists, then the bus cycle hangs. However, if the offset is in a chip-select or memory range, although the branch is to an improper address location, the error eventually recovers when the JMP instruction (at X-2) is executed in the operand execution pipeline.

To avoid this scenario, put a 128-byte space at the beginning and end of any code sections that might be affected by this sequence, so calculation of the improper target address does not impact system operation.

In addition, the assembly language for label or case statements as defined above can be modified to guarantee the problem does not occur. The use of the illegal opcode prior to the table of addresses prevents improper code re-direction. Note that the ColdFire ISA illegal opcode is different from the unknown, illegal opcodes referenced above. An example of the illegal opcode in a program is as follows:

```
      mov.l  (6,%pc,%d0.l*4),%a0 # offset changed to "6"
      jmp    (%a0)
      illegal                   # added instruction as workaround
label:
      long   label1
      long   label2
```

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3.1.2, 3-3

Add the following text:

If 16-bit MAC instruction operands are being used from different halves of different CPU registers, and if the V bit is being checked or if the MAC unit is operating in saturation mode, code modifications are required to ensure that the overflow logic works properly. For instance, mac.wRx:u,Ry:l should be replaced with the following equivalent sequence:

```
swap      Rx
mac.w     Rx:l,Ry:l
swap      Rx
```

mac.wRx:l,Ry:u should be replaced with the following sequence:

```
swap      Rx
mac.w     Rx:u,Ry:u
swap      Rx
```

Of course, the second swap instruction in each case should be removed if the MAC instruction specifies a memory operand that is to be loaded into the Rx register.

Similar sequences should be substituted for MSAC.W instructions.

The case for 16-bit operands from different halves of the same CPU register (y == x) is slightly more complicated. The instruction:

```
mac.w     Rx:u,Rx:l
```

should be replaced with:

```
      cmp.l     x,&0x80008000
      bne.b     label1
      mac.w     Rx:l,Rx:l
      bra.b     label2

label1:
      mac.w     Rx:u,Rx:l

label2:
```

Similar sequences should be used for MSAC.W instructions.

5.4.4, 5-11

In the description of the EMU bit, replace the bit description with the following text:

Do not set bit 13 of the debug module's Configuration/Status Register. The quickest entry into emulator mode after reset is created with the following sequence:

1.While in the BDM initiation sequence, program a debug breakpoint trigger event by an operand reference to address 0x0 or 0x4. As part of this sequence, the debug interrupt vector must also be initialized to the same address as the initial PC defined at address 4.

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	2.When the BDM GO command is received by the processor, the reset exception processing fetches the longwords at addresses 0 and 4 in normal mode and then a debug interrupt is immediately generated before the first instruction is executed. 3.Execution continues in emulator mode.
5.4.7, 5-14	Replace the last two sentences in the first paragraph with the following: Breakpoint logic can be configured as a single one-level trigger or a combination of one-level triggers. TDR[15:0] define the first-level trigger.
5.4.7, 5-15	Add the following text: NOTE: The second-level trigger does not work properly on the MCF5307. TDR[29:15] are effectively reserved bits.
5.4.7, 5-16	In the description for the DI bit, add the following text: Do not set DI for word or longword breakpoints.
5.6.1, 5-42	Add the following text: If debug interrupts are enabled, disable the capturing of operand writes because the stream of PST[3:0] = 0xD values may not be contiguous. Alternatively, ignore PST[3:0] = 0x0 values occurring during a debug interrupt. Let the debug interrupt exception processing be defined from the initial PST[3:0] = 0xD until PST[3:0] = 0x5.
6.2.10.1, 6-11	Table 6-6, PARK bit description, add the following text: NOTE: If round-robin mode (00) is selected, ensure that DCR[BWC] is set higher than the value in the BCR. If park-on-internal-DMA (10) or park-on-ColdFire-core (01) is selected, select DCR[BWC] = 000.
9.2.3, 9-6	Add the following text: NOTE: For interrupts sources with levels 1–6, write a higher level interrupt mask to the status register before setting the IMR. After the IMR is set, return the interrupt mask in the status register to its previous value. Do not mask a level-7 interrupt in the IMR. If these precautions are not followed, a spurious interrupt may occur.
11.4.2, 11-18	Add the following text: NOTE: Glitches may occur on the address lines unless EDGESEL is tied high or BCLKO is qualified with the assertion of $\overline{\text{SRAS}}$ or $\overline{\text{SCAS}}$ before connecting to the EDGESEL input. These glitches do not affect DRAM controller operation and are within the undershoot limits specified by Figure 1 of this document.
12.4.4, 12-9	Table 12-3, BWC bit description, add the following text: NOTE: Do not select the 000 encoding when MPARK[PARK]=00; the BWC encoding must be set higher than the value in the BCR in this mode. If MPARK[PARK]=10 or 01, BWC should equal 000.

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12.5.2.1, 12-13	Add the following text: NOTE: Use the CPU to write to the UART transmitter buffer. The DMA module is not able to properly transfer information from memory to the UART.
12.5.2.2, 12-13	Add the following text: Do not use single address access mode in cycle-steal mode; errant accesses may occur.
18.9, 18-23	Add the following text: NOTE: Either do not allow external master access to SDRAM using the MCF5307 DRAM controller or provide external termination for SDRAM bus cycles by an external master. The MCF5307 does not provide correct termination for external bus masters using the on-chip SDRAM controller.
20.1 20-2	Add the following diagram and text: Figure 1 shows the allowable undershoot voltage on the MCF5307. Note that 1.2-V undershoot is only allowable if it is present 1% or less of the total processor operating time.

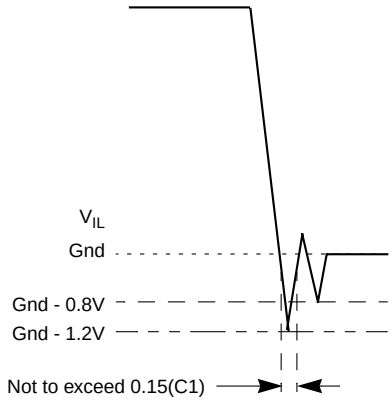

Figure 1. Undershoot Voltage

20.3 20-4	Make the following changes in Table 20-6: Change the Min specification for B14 to 2.0 nS for 66 MHz. Change the Min specification for B16 to 2.0 nS for 66 MHz.

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